REMARKS

Claims 1-24 are presently active.

In the Office Action dated 5 May 2003 ("Office Action"), claims 1, 15, and 24 were rejected under 35 U.S.C. §102(a) as being anticipated by Applicants' admitted prior art (Fig. 1); claims 2-7, 16, and 17-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' admitted prior art (Fig. 1); and claims 8-14 and 21-23 were allowed.

Applicants acknowledge with appreciation the allowance of claims 8-14 and 21-23.

35 U.S.C. §102(a) rejection of claims 1, 15, and 24

Written at the bottom of page 4 of the Office Action is the statement: "'Coupled to one another' includes being joined together, but is broader than that, in that two things are directly connected." Applicants agree. That is why "connected" is more narrow than "coupled". Claim 1 specifically recites "a NAND gate having a first input port connected to the node." This means that there is no intermediate device between the first input port and the node.

"Connected" cannot be interpreted as having the same scope as "coupled". For example, if one describes a circuit to one of ordinary skill in the art by saying "gate A is connected to node A," this would not mean that there is an active device or passive element interposed between gate A and node A.

The claim limitation of "a NAND gate having a first input port connected to the node" is simply not taught in Applicants' Fig. 1. Similar remarks apply to claim 24. Accordingly, Applicants' Fig. 1 does not teach all the claim limitations of claims 1 and 24, as well as claim 15 which depends upon claim 1, and therefore these claims are not anticipated by Applicants' Fig. 1.

35 U.S.C. §103(a) rejection of claims 2-7 and 16-20

Claims 2-4 depend upon claim 1. As discussed above, Applicants' Fig. 1 does not teach all of the claim limitations of claim 1. Nor does Applicants' Fig. 1 suggest the

claim limitation of "a NAND gate having a first input port connected to the node." Accordingly, claims 2-4 are not obvious in light of Applicants' Fig. 1.

To better define the invention, claim 5 is amended to recite that the NAND gate is a static NAND gate. The combination of pMOSFETs 112 and 114 cannot be identified with a static NAND gate. Accordingly, claim 5, and claims 6, 7, 18, 19, and 20 which depend upon claim 5, are not obvious in light of Applicants' Fig. 1.

Claim 16 depends upon claim 15. But as discussed above, Applicants' Fig. 1 does not teach all of the claim limitations of claim 15, and therefore it is believed that claim 16, and claim 17 which depends upon claim 16, are not obvious in light of Applicants' Fig. 1.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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John Patrick Ward
Registration No. 40,216

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 720-8300